What is Claimed is:

1. A device for converting a video format comprising:

a control unit for determining an operation conducted at the present time, recognizing an operation to be conducted at the next time based on the operation conducted at the present time, and providing control signals suitable for the operation to be conducted at the next time, according to an input video format of an input video signal and an output video format of an output video signal desired to provide; and,

a processing unit for conducting operations required for converting the input video format into the output video format desired to provide in response to the control signals form the control unit.

2. A device as claimed in claim 1, wherein the processing unit includes;

a first processing unit for converting a luminance signal format in the input video signal into a desired output video format,

a second processing unit for converting a chrominance signal format in the input video signal into a desired output video format, and

a separating unit for separating the received video signal into chrominance signals and a luminance signal.

3. A device as claimed in claim 2, wherein the first processing unit includes;

a delay for delaying a received luminance signal,

an operand mapping unit for utilizing the delayed luminance signal from the delay and a luminance signal received presently in determining initial operands to be used in a conversion

operation equation, i.e., a first value 'a' and a second value 'b', according to a format conversion ratio,

a numerator generating unit for generating a numerator in the conversion operation equation using the operands of the conversion operation equation from the operand mapping unit, and

a denominator generating unit for selecting a denominator of the conversion operation equation, dividing the numerator of the conversion operation equation from the numerator generating unit with the selected denominator, to obtain a converted luminance signal.

Sub a2 4. A device as claimed in claim 3, wherein the operand mapping unit includes;

a first multiplexer for providing a first value 'a', an initial operand, of the conversion operation equation according to a format conversion using the delayed luminance signal Y1 from the delay and a luminance signal Y2 received presently, and

a second multiplexer for providing a second value 'b', an initial operand, of the conversion operation equation according to a format conversion using the delayed luminance signal Y1 from the delay and a luminance signal Y2 received presently.

5. A device as claimed in claim 3, wherein the numerator generating unit includes;

a first shift left for shifting the first value 'a' from the first multiplexer to a left direction by units of an (n)th power of 2(2^n, n = 0, 1, 2, ---), to provide a plurality of values(a, 2a, 4a, 8a, ---) from the first value 'a', which are first intermediate operands,

a second shift left for shifting the second value 'b' from the second multiplexer to a left direction by units of an (n)th power of 2(2^n, n = 0, 1, 2, ---), to provide a plurality of values(b, 2b,

4b, 8b, ---) from the second value 'b', which are second intermediate operands, and

an operation processing unit for conducting operations required for obtaining the final operands and the numerators in the conversion operation equation from the first intermediate operands and the second intermediate operands.

6. A device as claimed in claim 5, wherein the operation processing unit includes;

a third multiplexer for receiving the values a, 2a, 4a, 8a from the first shift left and selecting and forwarding one of the values under the control of the control unit,

a fourth multiplexer for selectively providing either one of "a" and "0" from the first shift left under the control of the control unit,

a fifth multiplexer for selectively providing either one of values b, 2b, 4b, and 8b from the second shift left under the control of the control unit,

a sixth multiplexer for receiving the values 4b, 8b, and 16b from the second shift left and "0" and selectively providing any one of the received ones under the control of the control unit,

a seventh multiplexer for receiving the values b, 2b, and 4b from the second shift left and "0" and selectively providing any one of the received ones under the control of the control unit,

an operator for subjecting a value from the third multiplexer and a value from the fourth multiplexer to different operation as necessary,

a first adder for adding values from the fifth multiplexer and the first multiplexer,

a subtracter for subtracting a value from the seventh multiplexer from a value from the first adder, and

a second adder for adding values from the operator and the subtracter, to generate a numerator f1 of the conversion operation equation.

7. A device as claimed in claim 6, wherein the operator is either an adder or a subtracter.

8. A device as claimed in claim 3, wherein the denominator generating unit shifts the numerator f1 from the numerator generating unit by units of (n)th power(n=0, 1, 2, 3, ---) of 2 in a right direction, to provide a plurality of values ½, 1/4, 1/8, 1/16, --- (n=0, 1, 2, 3, ---), and

an operation processing unit for processing operations required for obtaining denominator of the conversion operation equation and a luminance signal having a final converted format using the plurality of values.

9. A device as claimed in claim 8, wherein the operation processing unit includes;

an eighth multiplexer for receiving the values f1, f1/2, and f1/4 from the shift right and providing one of the values under the control of the control unit,

a first divider for dividing a value from the eighth multiplexer by three,

a ninth multiplexer for selectively providing either one of a value f1 from the numerator generating unit and the value from the first divider,

a second divider for dividing a value from the ninth multiplexer by "five",

a third divider for dividing a value from the first divider by "three", and

a tenth multiplexer for selectively providing one of values from the first, second, and third dividers, a luminance signal Y2 received presently, and a value from the shift right as a converted luminance signal under the control of the control unit.

10. A device as claimed in claim 2, wherein the second processing unit includes;

a delay for delaying a chrominance signal,

an averaging unit for averaging a chrominance signal Cn-1 received presently and the chrominance signal delayed in the delay,

a first multiplexer for selectively providing either one of the chrominance signal received presently and a value from the averaging unit under the control of the control unit, and

a second multiplexer for selectively providing either one of the chrominance signal Cn delayed in the delay and a value from the averaging unit under the control of the control unit,

an operand mapping unit for utilizing the delayed luminance signal from the delay and a luminance signal received presently in determining initial operands to be used in a conversion operation equation, i.e., a first value 'a' and a second value 'b', according to a format conversion ratio,

a numerator generating unit for generating a numerator in the conversion operation equation using the operands of the conversion operation equation from the operand mapping unit, and

a denominator generating unit for selecting a denominator of the conversion operation equation, dividing the numerator of the conversion operation equation from the numerator generating unit with the selected denominator, to obtain a converted luminance signal.

11. A device as claimed in claim 10, wherein the operand mapping unit includes;

a third multiplexer for providing a first initial operand value 'a' of the conversion operation equation according to a format conversion using the signals from the first multiplexer and the second multiplexer, and

a fourth multiplexer for providing a second initial operand value 'b' of the conversion operation equation according to a format conversion using the signals from the first multiplexer

and the second multiplexer.

12. A device as claimed in claim 10, wherein the numerator generating unit includes;

a first shift left for shifting the value 'a' from the third multiplexer to a left direction by units of an (n)th power of 2(2^n, n = 0, 1, 2, ---), to provide a plurality of values(a, 2a, 4a, 8a, ---) from the value 'a', which are first intermediate operands,

a second shift left for shifting the value 'b' from the fourth multiplexer to a left direction by units of an (n)th power of 2(2^n, n = 0, 1, 2, ---), to provide a plurality of values(b, 2b, 4b, 8b, ---) from the value 'b', which are second intermediate operands, and

an operation processing unit for conducting operations required for obtaining the final operands and the numerators in the conversion operation equation from the first intermediate operands and the second intermediate operands.

13. A device as claimed in claim 12, wherein the operation processing unit includes;

a third multiplexer for receiving the values a, 2a, 4a, 8a from the first shift left and selecting and forwarding one of the values under the control of the control unit,

a fourth multiplexer for selectively providing either one of "a" and "0" from the first shift left under the control of the control unit,

a fifth multiplexer for selectively providing either one of values b, 2b, 4b, and 8b from the second shift left under the control of the control unit,

a sixth multiplexer for receiving the values 4b, 8b, and 16b from the second shift left and "0" and selectively providing any one of the received ones under the control of the control unit,

a seventh multiplexer for receiving the values b, 2b, and 4b from the second shift left and

"0" and selectively providing any one of the received ones under the control of the control unit,

an operator for subjecting a value from the third multiplexer and a value from the fourth multiplexer to different operation as necessary,

a first adder for adding values from the fifth multiplexer and the first multiplexer,

a subtracter for subtracting a value from the seventh multiplexer from a value from the first adder, and

a second adder for adding values from the operator and the subtracter, to generate a numerator f1 of the conversion operation equation.

14. A device as claimed in claim 13, wherein the operator is either an adder or a subtracter.

15. A device as claimed in claim 10, wherein the denominator generating unit shifts the numerator f1 from the numerator generating unit by units of (n)th power(n=0, 1, 2, 3, ---) of 2 in a right direction, to provide a plurality of values ½, 1/4, 1/8, 1/16, --- (n=0, 1, 2, 3, ---), and

an operation processing unit for processing operations required for obtaining denominator of the conversion operation equation and a luminance signal having a final converted format using the plurality of values.

16. A device as claimed in claim 15, wherein the operation processing unit includes;

an eighth multiplexer for receiving the values f1, f1/2, and f1/4 from the shift right and providing one of the values under the control of the control unit,

a first divider for dividing a value from the eighth multiplexer by three,

a ninth multiplexer for selectively providing either one of a value f1 from the numerator generating unit and the value from the first divider,

a second divider for dividing a value from the ninth multiplexer by "five",

a third divider for dividing a value from the first divider by "three", and

a tenth multiplexer for selectively providing one of values from the first, second, and third dividers, a chrominance signal Y2 received presently, and a value from the shift right as a converted chrominance signal under the control of the control unit.

17. A digital television receiver, comprising:

an antenna;

a tuner for synchronizing to a desired channel signal;

an intermediate frequency signal generating unit for generating an intermediate frequency signal of the synchronized channel signal;

an audio signal processing unit for processing an audio signal only in the intermediate frequency signal so that the audio signal is audible;

a video signal processing unit for processing a video signal only in the intermediate frequency signal for obtaining chrominance signals and a luminance signal;

a filter unit for low pass filtering the video signal from the video signal processing unit;

a vertical format converting unit for converting a video signal format from the filter unit in a vertical direction to match to a desired output signal format; and,

a horizontal format converting unit for converting a video signal format from the vertical format converting unit in a horizontal direction to match to a desired output video signal format, wherein each of the vertical format converting unit and the horizontal format converting unit

includes;

a control unit for determining an operation conducted at the present time, recognizing an operation to be conducted at the next time based on the operation conducted at the present time, and providing control signals suitable for the operation to be conducted at the next time, according to an input video format of an input video signal and an output video format of an output video signal desired to provide,

a first processing unit for converting a luminance signal format in the input video signal into a desired output video format,

a second processing unit for converting a chrominance signal format in the input video signal into a desired output video format, and

a separating unit for separating the received video signal into chrominance signals and a luminance signal.

18. A device as claimed in claim 17, wherein the first processing unit includes;

a delay for delaying a received luminance signal,

an operand mapping unit for utilizing the delayed luminance signal from the delay and a luminance signal received presently in determining initial operands to be used in a conversion operation equation, i.e., a first value 'a' and a second value 'b', according to a format conversion ratio,

a numerator generating unit for generating a numerator in the conversion operation equation using the operands of the conversion operation equation from the operand mapping unit, and

a denominator generating unit for selecting a denominator of the conversion operation

equation, dividing the numerator of the conversion operation equation from the numerator generating unit with the selected denominator, to obtain a converted luminance signal.

19. A device as claimed in claim 18, wherein the operand mapping unit includes;

a first multiplexer for providing a first value 'a', an initial operand, of the conversion operation equation according to a format conversion using the delayed luminance signal Y1 from the delay and a luminance signal Y2 received presently, and

a second multiplexer for providing a second value 'b', an initial operand, of the conversion operation equation according to a format conversion using the delayed luminance signal Y1 from the delay and a luminance signal Y2 received presently.

20. A device as claimed in claim 18, wherein the numerator generating unit includes;

a first shift left for shifting the first value 'a' from the first multiplexer to a left direction by units of an (n)th power of 2(2^n, n = 0, 1, 2, ---), to provide a plurality of values(a, 2a, 4a, 8a, ---) from the first value 'a', which are first intermediate operands,

a second shift left for shifting the second value 'b' from the second multiplexer to a left direction by units of an (n)th power of 2(2^n, n = 0, 1, 2, ---), to provide a plurality of values(b, 2b, 4b, 8b, ---) from the second value 'b', which are second intermediate operands, and

an operation processing unit for conducting operations required for obtaining the final operands and the numerators in the conversion operation equation from the first intermediate operands and the second intermediate operands.

21. A device as claimed in claim 18, wherein the denominator generating unit shifts the

numerator f1 from the numerator generating unit by units of (n)th power(n=0, 1, 2, 3, ---) of 2 in a right direction, to provide a plurality of values ½, 1/4, 1/8, 1/16, --- (n=0, 1, 2, 3, ---), and

an operation processing unit for processing operations required for obtaining denominator of the conversion operation equation and a luminance signal having a final converted format using the plurality of values.

22. A device as claimed in claim 17, wherein the second processing unit includes;

a delay for delaying a chrominance signal,

an averaging unit for averaging a chrominance signal Cn-1 received presently and the chrominance signal delayed in the delay,

a first multiplexer for selectively providing either one of the chrominance signal received presently and a value from the averaging unit under the control of the control unit, and

a second multiplexer for selectively providing either one of the chrominance signal Cn delayed in the delay and a value from the averaging unit under the control of the control unit,

an operand mapping unit for utilizing the delayed luminance signal from the delay and a luminance signal received presently in determining initial operands to be used in a conversion operation equation, i.e., a first value 'a' and a second value 'b', according to a format conversion ratio,

a numerator generating unit for generating a numerator in the conversion operation equation using the operands of the conversion operation equation from the operand mapping unit, and

a denominator generating unit for selecting a denominator of the conversion operation equation, dividing the numerator of the conversion operation equation from the numerator

generating unit with the selected denominator, to obtain a converted luminance signal.

23. A device as claimed in claim 17, further comprising a ratio detecting unit for detecting a format conversion ratio from an input video format to an output video format and providing the detected format conversion ratio to the vertical format converting unit and the horizontal format converting unit.